3. (Amended) An integrated circuit, comprising:

a first circuit section formed in a substrate;

a second circuit section formed in the substrate, the second circuit section being spaced laterally from the first circuit section;

an isolation buried layer formed under at least a portion of the first circuit section; and

a conductive layer formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer at a plurality of points spaced throughout the buried layer, the conductive layer reducing an effective lateral resistance of the isolation buried layer to thereby increase an electrical isolation between the first and second circuit sections;

wherein the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net.

4. (Amended) The integrated circuit of claim 1, wherein the net includes a plurality of holes therein, at least a portion of the first circuit section being formed in one or more holes in the net.

5. (Amended) The integrated circuit of claim 1, wherein the net overlays at least a portion of the first circuit section.

6. (Amended) The integrated circuit of claim 30, wherein the isolation buried layer is connected to a ground or reference source.

7. (Amended) The integrated circuit of claim 30, wherein the conductive layer is formed at least in part of metal.

8. (Amended) The integrated circuit of claim 30, further comprising:

a second isolation buried layer formed under at least a portion of the second circuit section; and

a second conductive layer formed on a surface of the integrated circuit and operatively coupled to the second isolation buried layer, the second conductive layer reducing an effective lateral resistance of the second isolation buried layer.

15. (Amended) The integrated circuit of claim 30, wherein:

the integrated circuit is a mixed signal integrated circuit;

the first circuit section comprises a digital circuit section; and

the second circuit section comprises an analog circuit section.

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16. (Amended) The integrated circuit of claim 30, wherein the isolation buried layer has a lower resistivity than the substrate.

17. (Amended) The integrated circuit of claim 30, wherein the isolation buried layer is formed in the substrate at depth in a range from about 2 micrometers (μm) to about 5 μm from an upper surface of the substrate.